

BINGHAM McCUTCHEON

# Facsimile

DATE January 9, 2004

	NAME	FAX	PHONE
Bingham McCutchen LLP 1900 University Avenue East Palo Alto, CA 94303-2223	<b>TO</b> Examiner Matthew C. Dooley United States Patent and Trademark Office	703-746-8183	703-306-5538
650.849.4400 650.849.4800 fax	<b>FROM</b> Jeffrey S. Smith jeffrey.smith@bingham.com	(650) 849-4800	(650) 849-4422
bingham.com	<b>PAGES</b> (INCLUDING THIS COVER PAGE): 6		
Boston Hartford London  Los Angeles New York Orange County San Francisco Silicon Valley  Tokyo Walnut Creek Washington	<b>RE</b> U.S. Application Serial No.: 09/765,958		
<b>MESSAGE</b>			

Per our conversation this morning. Please confirm receipt of this fax by return fax or call Sheila Henriquez @ 650-849-4455, or email at sheila.henriquez@bingham.com.

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DATE April 22, 2003

	NAME	FAX	PHONE
TO	Examiner Magid Dimyan U.S. Patent & Trademark Office	703/872-9318	

FROM Jeffrey S. Smith (650) 849-4800 (650) 849-4422  
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PAGES (INCLUDING THIS COVER PAGE): 4

RE U.S. Serial No. 09/765,958

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H 6 1/2 / 1-14-04  
A ✓ Gene

Appl. No. 09/765,958

261/085

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application No.: 09/765,958  
Applicant: Bulent Dervisoglu, Laurence H. Cooke  
Filing Date: 1/18/01  
Title: Hierarchical Test Circuit Structure for Chips with Multiple Circuit Blocks  
Assignee: Cadence Design Systems, Inc.  
Examiner: Magid Dimyan  
Group Art Unit: 2857  
Docket No.: 261/085

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Commissioner for Patents  
Washington, D.C. 20231

**PRELIMINARY AMENDMENT**

Sir:

Before examination on the merits, please amend this application as follows:

**Amendments to the Claims** are reflected in the listing of claims which begins on page 2 of this paper.

**Remarks** begin on page 3 of this paper.